PCT

WORLD INTELLECTUAL PROPERTY ORGANIZATION
International Bureau

INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 4 : B44C 1/22, H01L 21/00

A1

(11) International Publication Number: WO 90/00476

(43) International Publication Date: 25 January 1990 (25.01.90)

(21) International Application Number: PCT/US89/02929

(22) International Filing Date: 10 July 1989 (10.07.89)

(30) Priority data:
217,915 12 July 1988 (12.07.88) US

(71) Applicant: THE REGENTS OF THE UNIVERSITY OF CALIFORNIA [US/US]; 300 Lakeside Drive, 22nd Floor, Oakland, CA 94612-3550 (US).

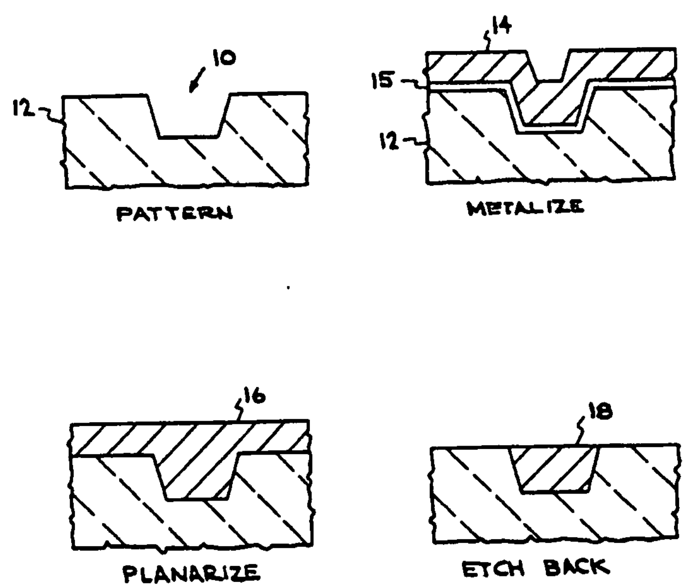
(72) Inventor: TUCKERMAN, David, B. ; 5228 Felicia Avenue, Livermore, CA 94550 (US).

(74) Agents: EGAN, William, J. et al.; Flehr, Hohbach, Test, Albritton & Herbert, Four Embarcadero Center, Suite 3400, San Francisco, CA 94111-4187 (US).

(81) Designated States: AT (European patent), BE (European patent), CH (European patent), DE (European patent), FR (European patent), GB (European patent), IT (European patent), JP, KR, LU (European patent), NL (European patent), SE (European patent).

Published
With international search report.

(54) Title: PLANARIZED INTERCONNECT ETCHBACK



(57) Abstract

In a process for fabricating planarized thin film metal interconnects (18) for integrated circuit structures, a planarized metal layer (14) is etched back to the underlying dielectric layer (12) by electropolishing, ion milling or other procedure. Electropolishing reduces processing time from hours to minutes and allows batch processing of multiple wafers (22, 30). The etched back planarized thin film interconnect (18) is flush with the dielectric layer (12).

PLANARIZED INTERCONNECT ETCHBACK

The United States Government has rights in this invention pursuant to Contract No. W-7405-ENG-48 between the U. S. Department of Energy and the University of California, for the operation of Lawrence Livermore National Laboratory.

BACKGROUND OF THE INVENTION

The invention relates generally to planarized interconnects for integrated circuit structures and more particularly to the formation of fully planarized interconnects.

U.S. Patents 4,674,176 and 4,681,795 to Tuckerman describe thin film metal layer planarization processes for multilevel interconnect. In the fabrication of multilevel integrated circuit structures, the planarization of each metal layer eliminates irregular and discontinuous conditions between successive layers, particularly where vias are located.

The metal layer is planarized by heating for a brief, controlled time related to the spatial period of the features to be planarized. The entire planarization process, for forming the planarized interconnect, includes forming a thin film metal layer on a dielectric layer, and briefly heating the metal layer to produce a flat surface on the metal layer. An additional dielectric layer can then be deposited and the process repeated as many times as necessary to produce the required number of levels. However, in order to achieve fully planar multilevel interconnects, it is still necessary to planarize the dielectric layer.

Thus it is desirable to develop a planarization process in which dielectric planarization is unnecessary. This can be achieved by fabricating planarized metal interconnects which are flush with the dielectric layers. It is also desirable to develop a process in which further processing time is rapid and in which multiple interconnects can be processed simultaneously in a batch process.

SUMMARY OF THE INVENTION

Accordingly, it is an object of the invention to provide an improved method of forming a thin film planarized metal interconnect which does not require any

dielectric planarization.

It is also an object of the invention to provide an improved planarization process which is very rapid and can process multiple wafers simultaneously.

It is another object of the invention to provide an improved thin film planarized metal interconnect.

It is a further object of the invention to provide an improved thin film planarized metal interconnect which is flush with the surrounding dielectric layer.

The invention is a method of fabricating planarized thin film metal interconnects in which the planarized metal layer is etched back to the surrounding dielectric layer, preferably by electropolishing; the invention also includes the resulting etched back planarized interconnect. A dielectric layer is first patterned or etched to form either a trench for the metal interconnect or a via to an underlying metal layer or a combination of a trench and a via, and then metallized or coated with an adhesion layer (if necessary) and a metal layer which, to some extent, follows the surface contours of the etched dielectric layer. The metal layer is then planarized to form a metal layer with a substantially flat surface which fills the trench and extends over the dielectric layer. The flat metal layer is then etched

back to the level of the dielectric layer by electropolishing or ion milling or other etchback techniques, leaving a metal interconnect with a flat surface filling the trench or via and flush with the dielectric surface. The electropolishing can be carried out rapidly in a batch process in which a plurality of wafers on which planarized metal layers have been formed are electrically connected to a voltage source and placed in an electropolishing solution. In addition to performing the etchback, the electropolishing may also further planarize the metal layer. The etchback can be performed in minutes by electropolishing.

BRIEF DESCRIPTION OF THE DRAWINGS

In the accompanying drawings:

Figures 1A-D illustrate a process for forming a planarized metal layer for an interconnect, including etching back the planarized layer.

Figure 2 is a perspective cutaway view of a planarized etched back interconnect structure formed with trenches, vias, and combinations thereof.

Figure 3 illustrates an electropolishing apparatus for performing etchback of wafers with planarized metal layers.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

A method for fabricating planarized thin film metal interconnects for integrated circuits, and the resulting structures, is illustrated in Figures 1A-D. A trench or via 10 is etched or otherwise formed in a dielectric layer 12, typically made of SiO_2, of a circuit structure, at the location where a metal interconnect is to be formed. The etched or patterned dielectric layer 12, including trench 10, is then coated by conventional methods such as sputtering or electroplating with an adhesion layer 15 (if necessary), followed by a metal layer 14 which substantially follows the surface contours of the etched dielectric layer and fills the trench. The metal layer is typically about 1 to 5 microns thick and made of gold, copper, silver, or aluminum. The adhesion layer is typically titanium or chromium. Metal layer 14 is then planarized, e.g. by pulsed laser pulses, to form a substantially flat metal layer 16 which completely fills the trench and extends over the dielectric layer. The planarization step is performed by controlled heating and melting of the metal layer, using lasers or other pulsed energy sources, for a time related to the spatial period of the features being planarized, as further described to U.S. Patents 4,674,176 and 4,681,795, which are herein incorporated by reference.

In order to remove the metal above the dielectric layer so that the metal interconnect is flush with the surface of the dielectric layer, the planarized metal layer 16 is etched back to the dielectric layer to form an etched back thin film metal interconnect 18. In a preferred embodiment of the invention, the etchback is performed by electropolishing. The metal layer to be etched back is made the anode in an electric circuit. The metal is placed in an electrolytic bath and an electric current is run through the bath to cause anodic dissolution of the metal layer. The etchback step can also be performed by ion milling or other processes. However, the ion milling etchback step is very time consuming, often greater than one hour per wafer. Also only one wafer can generally be processed at a time by ion milling.

To form multilevel interconnects, an additional layer of dielectric is formed over the structure of Figure 1D and the process is repeated.

Although the invention has been described with respect to planarizing and etching back a metal interconnect in a trench formed in a dielectric layer, the invention is also applicable to the formation of interconnects through vias (holes) extending through a dielectric layer to an underlying metal layer, or to a

combination of a trench with vias extending therefrom to an underlying metal layer. In each case, the dielectric layer is first patterned with the appropriate trenches, vias, or combinations thereof; the patterned dielectric layer is then metallized, planarized, and etched back to form the interconnect.

The various types of interconnect structures are illustrated in Figure 2. A trench 33 is formed in a dielectric layer 34. Dielectric layer 34, including trench 33, are then coated with metal, which is then planarized and etched back to the surface 36 of dielectric layer 34, forming a metal interconnect 32 in trench 33 which is flush with the surface 36 of dielectric layer 34. An additional dielectric layer 38 is formed on layer 34 and vias 40, 42 are formed through dielectric layer 38 to underlying metal interconnect 32; the dielectric layer 38, including vias 40, 42, are then metallized. The metallization is planarized and etched back to the surface 44 of dielectric layer 38, forming solid plugs of metal 41, 43, respectively, within vias 40, 42 which are flush with the surface 44. Another dielectric layer 46 with a trench 49 is formed on dielectric layer 38, and a metal layer is deposited, planarized, and etched back to form an interconnect 48 in trench 49 which is flush with the surface 50 and which contacts plugs 41, 43 in vias 40, 42.

Dielectric layers 38, 46 may be formed as a single layer on dielectric layer 34, and the single layer patterned with a trench 49 extending partly though the single dielectric layer (corresponding to upper layer 46) and with vias 40, 42 from the trench 49 to the underlying metal interconnect 32. The combination trench and vias are then metallized in a single operation, and the metal interconnect is planarized and etched back to upper surface 50.

An electropolishing apparatus 20 for carrying out the etchback of planarized metal layers on wafers in a batch process is illustrated in Figure 3. A plurality of wafers 22 are placed in a tank 24 filled with electroplating solution (electrolyte) 26 and connected to the positive terminal (anode) of an applied DC voltage source 28 while electrodes 30, which resist chemical interaction with the electrolyte, e.g. carbon, are connected to the negative terminals. The electrolyte is often an acid. Source 28 produces the required current density for the particular metal. Gold, silver, copper and aluminum can all be electropolished. The electropolishing performs not only the etchback step but in some cases may further planarize the metal layer if the initial planarization was incomplete. The operator halts the electropolishing as soon as the metal is removed from

the main (non-trenched) areas of the dielectric layers, leaving only an adhesion layer (if present) on the main areas. This adhesion layer may be removed by wet chemical etching. The remaining metal interconnect is in the trenches and is flush with the dielectric surface.

Planarization is desirable to form thick multilevel metal interconnects of high integrity. Performing the etchback by electropolishing reduces processing time from hours to minutes.

Changes and modifications in the specifically described embodiments can be carried out without departing from the scope of the invention which is intended to be limited only by the scope of the appended claims.

CLAIMS

1. Method of forming a planarized thin film metal interconnect in a dielectric layer on an integrated circuit wafer, comprising:

forming a trench or via in the dielectric layer for the metal interconnect;

depositing a metal layer on the dielectric layer;

planarizing the metal layer to form a metal layer with a substantially flat surface which fills the trench or via and extends over the surrounding dielectric layer;

etching back the flat metal layer to the dielectric layer.

2. The method of Claim 1 wherein the metal is etched back by electropolishing.

3. The method of Claim 1 wherein the metal is etched back by ion milling.

4. The method of Claim 1 wherein the trench or via is formed in the dielectric layer by etching.

5. The method of Claim 1 wherein the planarization of the metal layer is performed by controlled heating and melting of the metal layer for a time related to the spatial period of the features being planarized.

6. The method of Claim 5 wherein the controlled heating and melting is performed by applying pulsed energy to the metal layer.

7. The method of Claim 6 comprising applying laser pulses.

8. The method of Claim 1 further comprising forming the metal layer of gold, silver, copper, or aluminum.

9. The method of Claim 1 further comprising forming the metal layer with a thickness in the range of about 1 to 5 microns.

10. The method of Claim 2 wherein the etching back by electropolishing is performed by:

connecting the wafer to the anode of a DC voltage source;

placing the wafer in an electrolyte;

flowing a DC current of sufficient current density through the wafer.

11. The method of Claim 2 further comprising performing the etching back by electropolishing on a plurality of wafers simultaneously.

12. The method of Claim 1 further comprising forming an additional dielectric layer over the etched back metal interconnect and repeating the steps of forming a trench or via, depositing a metal layer, planarizing the metal layer and etching back the metal layer to form a multilevel interconnect.

13. The method of Claim 12 wherein the metal layer is etched back by electropolishing.

14. The method of Claim 12 wherein the metal layer is etched back by ion milling.

15. In an integrated circuit structure, a metal interconnect comprising an etched back planarized thin film metal interconnect formed in a dielectric layer of the circuit structure and having a planarized flat surface which is flush with the dielectric layer.

16. The etched back metal interconnect of Claim 15 wherein the metal interconnect is formed of gold, copper, silver, or aluminum.

17. The etched back metal interconnect of Claim 15 wherein the metal interconnect has a thickness of about 1-5 microns.

18. The etched back metal interconnect of Claim 15 arranged in a multilevel interconnect.

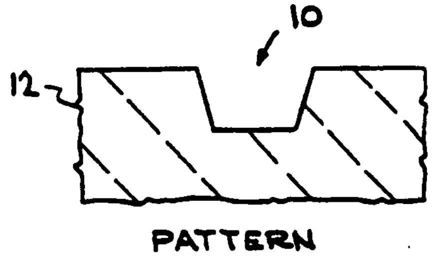


FIG. 1A

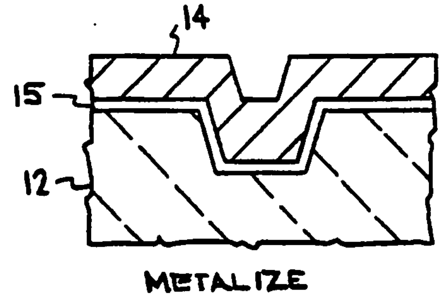


FIG. 1B

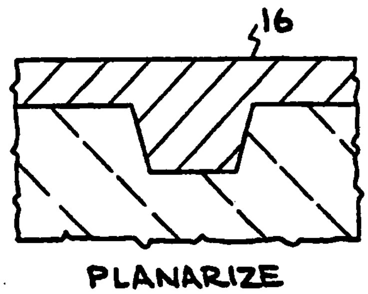


FIG. 1C

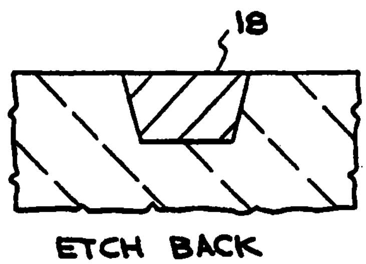


FIG. 1D

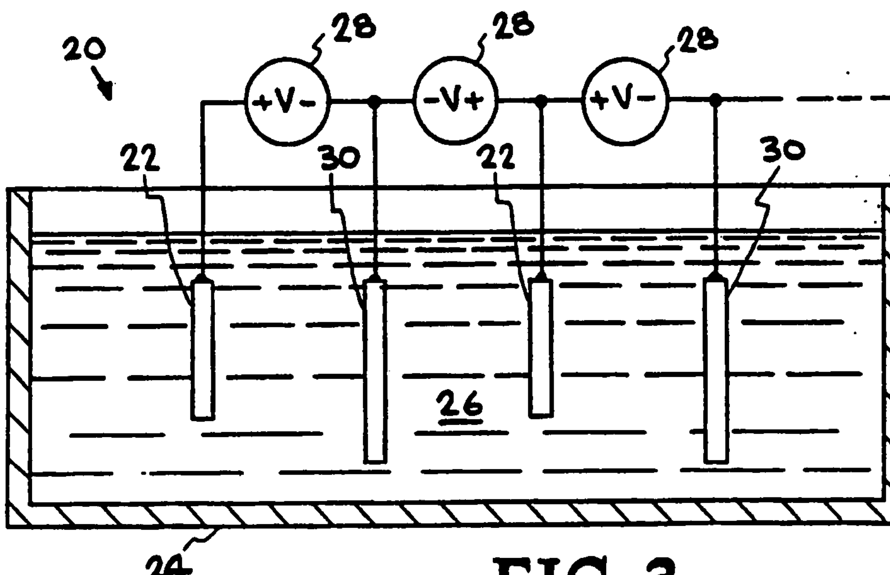


FIG. 3

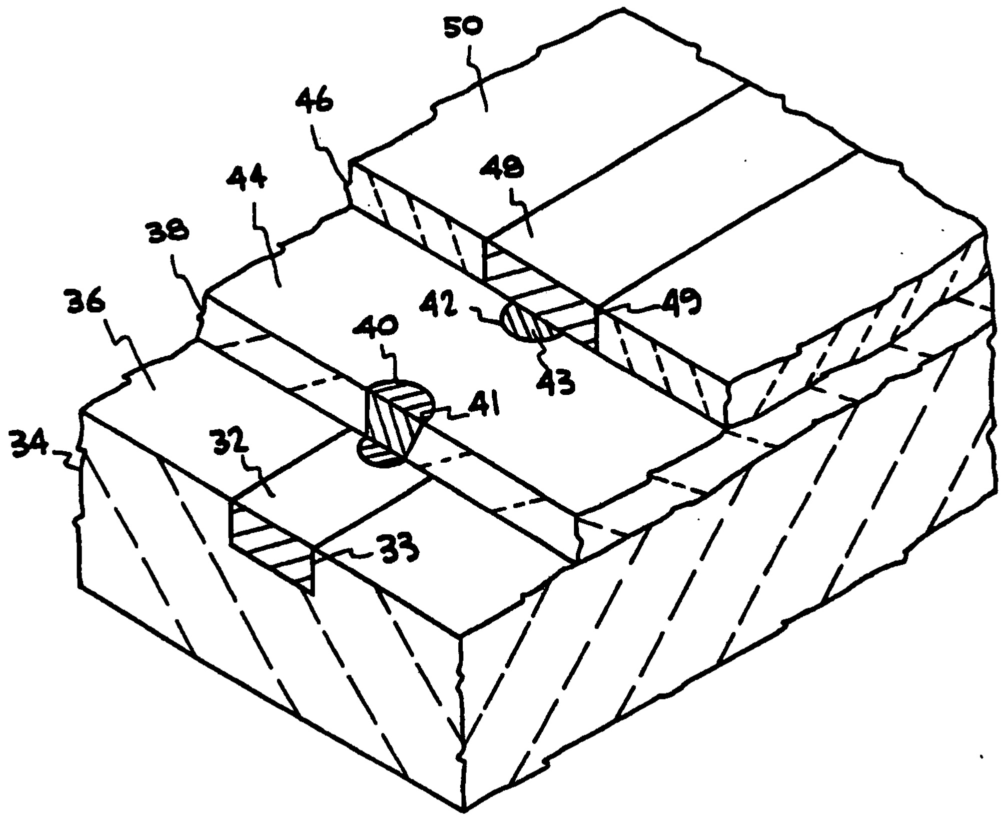


FIG. 2

INTERNATIONAL SEARCH REPORT

International Application No. PCT/US89/02929

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all) [6]

According to International Patent Classification (IPC) or to both National Classification and IPC

IPC(4): B44C 1/22; H01L 21/00

U.S.CL.: 156/656, 657, 662; 437/203; 204/129.1

II. FIELDS SEARCHED

Minimum Documentation Searched [7]

Classification System	Classification Symbols
U.S.	156/656, 657, 662; 437/203; 204/129.1

Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched [8]

III. DOCUMENTS CONSIDERED TO BE RELEVANT [9]

Category [*]	Citation of Document, [11] with indication, where appropriate, of the relevant passages [12]	Relevant to Claim No. [13]
Y	US, A, 4,708,767 (BRIL) 24 November 1987 See the entire document.	1,3-9,12,14
Y,P	US, A, 4,800,179 (MUKAI) 24 January 1989 See the entire document.	1-14
X / Y	US, A, 3,849,270 (TAKAGI et al) 19 November 1974 See the entire document.	15-18 / 1,2,4-13

* Special categories of cited documents: [10]

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

IV. CERTIFICATION

Date of the Actual Completion of the International Search	Date of Mailing of this International Search Report
08 August 1989	02 OCT 1989
International Searching Authority	**Signature of Authorized Officer**
ISA/US	Thi Dang THI DANG